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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,238	12/05/2000	Brian A. Leete	884.335US1	7903

21186 7590 09/08/2004

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EXAMINER

LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/730,238	<b>Applicant(s)</b> LEETE, BRIAN A.	
	<b>Examiner</b> Christopher E. Lee	<b>Art Unit</b> 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 June 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 and 26-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 and 26-48 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/18/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Receipt Acknowledgement***

1. Receipt is acknowledged of the Amendment filed on 18<sup>th</sup> of June 2004. Claims 1, 7, 11, 12 and 18 have been amended; no claim has been canceled; and claims 28-48 have been newly added since the RCE Non-Final Office Action was mailed on 13<sup>th</sup> of April 2004. Currently, claims 1-23 and 26-48 are pending in this application.

### ***Information Disclosure Statement***

2. The Applicant submitted information disclosure statement (IDS) on 18<sup>th</sup> of June 2004 was filed, but the foreign patent document JP-2000231969 to Yaguchi has not been reconsidered because the foreign patent document JP-2000231969 was made of record by the Examiner on the Non-Final Office Action mailed on 20<sup>th</sup> of June 2003, and its full English translation was provided to the Applicant on the Final Office Action mailed on 24<sup>th</sup> of December 2003 under the condition of the following notice. Notice : The Examiner referred to Yaguchi et al. [JP 2000231969] reference as a prior art for the claim rejections in the prior Office Action, and it was referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attached a machine translated copy of the reference for the convenience of the Applicant. However, the Examiner cautioned the Applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

### ***Claim Objections***

3. Claims 7, 11 and 18 are objected to because of the following informalities:

In each of the claims 7, 11 and 18, the claim status is not indicated in a parenthetical expression.

See MPEP 714 [R-2] and 37 CFR 1.121(c). Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-4, 7, 11, 12, 16, 17, 19, 28-32, 39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A].

*Referring to claim 1*, Herwig discloses an apparatus (i.e., wiring Hub 100 of Fig. 3), comprising: a housing (i.e., housing 110 of Fig. 3); a power supply (i.e., Power Supply 112 of Fig. 3) enclosed in said housing (See Fig. 3); a bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) enclosed in said housing (See Fig. 3); and a downstream receptacle (i.e., cable connector between lines 136, 138 and lines 90, 94 in Fig. 3) connected to both said power supply and said bus hub (i.e., line 138 connected to Power Supply 112 and line 136 connected to Protocol Conversion & USB Hub 114 in Fig. 3), said downstream receptacle being coupled to a cable (i.e., line 136 and line 138 in Fig. 3) to couple power from said power supply (See col. 6, lines 65-66) and data signals from said bus hub to said cable (See col. 7, lines 11-15) and to receive power and data signals from said cable (See col. 6, line 65 through col. 7, line 10). Herwig does not expressly teach said power supply being coupled to said bus hub to supply power to said bus hub.

Flannery discloses an apparatus of providing power management using a self-powered USB device (See Abstract and Fig. 1A), wherein said apparatus comprising a power logic 114 (Fig. 1A) and a power supply (i.e., power supply 108 of Fig. 1A) being coupled to a bus hub (i.e., HUB Logic 106 of Fig. 1) to supply power to said bus hub (See col. 5, line 65 through col. 6, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus of providing power management, as disclosed by Flannery, to said apparatus, as disclosed by Herwig, so as to provide a superior solution to supplying the power needs of suspend/resume capabilities in a computer without the inefficiencies of a dual-stage power supply unit or

the expense of incorporating both low-power and full-power units (See Flannery, col. 2, line 62 through col. 3, line 2) with the advantage of being able to supply 500mA to each downstream device (e.g., printers and speakers) attached to said bus hub (See Flannery, col. 4, lines 50-64).

*Referring to claim 11*, Herwig teaches that said power supply (i.e., Power Supply 112 of Fig. 3) is coupled to a wire (i.e., power cord 102 of Fig. 3) to receive alternating current (AC) power (i.e., 110V AC), said power supply to convert said AC power into direct current (DC) power (i.e., 5/12 DC; See col. 6, lines 51-64).

*Referring to claim 12*, Herwig discloses a computing unit (i.e., retail terminal system 50 in Fig. 2), comprising: a computer (i.e., main unit 52 of Fig. 2) comprising: an upstream receptacle (i.e., cable connector between line 94 and input device 55 in Fig. 2) to deliver data signals (i.e., USB data signals) to said computer (See col. 7, lines 11-15); and a power receptacle (i.e., cable connector between line 90 and input device 55 in Fig. 2) to deliver electrical power (i.e., terminal power) to said computer (See col. 6, lines 65-67); and a power hub (i.e., wiring Hub 100 of Fig. 3) coupled to said upstream receptacle and said power receptacle via a cable (i.e., line 136 and line 138 in Fig. 3; See col. 6, line 65 through col. 7, line 10), wherein said power hub (i.e., wiring Hub) comprises: a housing (i.e., housing 110 of Fig. 3); a power supply (i.e., Power Supply 112 of Fig. 3) enclosed in said housing (See Fig. 3), said power supply being coupled to said cable to provide power to said computer (See col. 6, line 65 through col. 7, line 10); and a bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) enclosed in said housing (See Fig. 3), said bus hub being coupled to said cable (i.e., Protocol Conversion & USB Hub 114 of Fig. 3 being coupled to Power & LAN 90 and USB interface 94, viz., cable, in Fig. 2) to receive power (i.e., receiving Vbus power via USB interface 94 of Fig. 2) and data signals (i.e., receiving D+, D- data signals via USB interface 94 of Fig. 2) from said computer (i.e., main unit).

Herwig does not expressly teach said power supply being coupled to said bus hub to supply power to said bus hub.

Flannery discloses an apparatus of providing power management using a self-powered USB device (See Abstract and Fig. 1A), wherein said apparatus comprising a power logic 114 (Fig. 1A) and a power supply (i.e., power supply 108 of Fig. 1A) being coupled to a bus hub (i.e., HUB Logic 106 of Fig. 1) to supply power to said bus hub (See col. 5, line 65 through col. 6, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus of providing power management, as disclosed by Flannery, to said computing unit, as disclosed by Herwig, so as to provide a superior solution to supplying the power needs of suspend/resume capabilities in a computer without the inefficiencies of a dual-stage power supply unit or the expense of incorporating both low-power and full-power units (See Flannery, col. 2, line 62 through col. 3, line 2) with the advantage of being able to supply 500mA to each downstream device (e.g., printers and speakers) attached to said bus hub (See Flannery, col. 4, lines 50-64).

*Referring to claims 2 and 16*, Herwig teaches said bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) comprises an upstream port (i.e., port from Protocol Conversion & USB Hub 114 for line 136 in Fig. 3).

*Referring to claims 3 and 17*, Herwig teaches said bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) comprises at least one downstream port (i.e., USB Port #1 140 and USB Port #2 142 in Fig. 3) to connect to at least one downstream device (e.g., Scanner 66 and POS Keyboard 62 in Fig. 2).

*Referring to claims 4 and 19*, Flannery teaches said bus hub (i.e., HUB Logic 106 of Fig. 1A) is self powered (See col. 5, lines 64-66).

*Referring to claim 7*, Herwig, as modified by Flannery, teaches that said power supply (i.e., Power Supply 112 of Fig. 3; Herwig) is coupled to a wire (i.e., power cord 102 of Fig. 3; Herwig) to receive alternating current (AC) power (i.e., 110V AC; Herwig) to convert said AC power into direct current (DC) power (i.e., 5/12 DC; See Herwig, col. 6, lines 51-64), said DC power being coupled to said

downstream receptacle (i.e., cable connector between lines 136, 138 and lines 90, 94 in Fig. 3; Herwig) and to said bus hub (i.e., HUB Logic 106 of Fig. 1A; Flannery).

*Referring to claim 28*, Herwig, as modified by Flannery, teaches that said power supply (i.e., Power Supply 112 of Fig. 3; Herwig) is coupled to receive alternating current (AC) power (i.e., 110V AC; Herwig) to convert said AC power into direct current (DC) power (i.e., 5/12 DC; See Herwig, col. 6, lines 51-64), said DC power being coupled to said (i.e., cable connector between lines 136, 138 and lines 90, 94 in Fig. 3; Herwig) and to said bus hub (i.e., HUB Logic 106 of Fig. 1A; Flannery).

*Referring to claim 29*, Herwig discloses an apparatus (i.e., wiring Hub 100 of Fig. 3), comprising: a housing (i.e., housing 110 of Fig. 3); a power supply (i.e., Power Supply 112 of Fig. 3) enclosed in said housing (See Fig. 3), said power supply (i.e., Power Supply 112 of Fig. 3) being coupled to receive alternating current (AC) power (i.e., 110V AC) to convert said AC power into direct current (DC) power (i.e., 5/12 DC; See col. 6, lines 51-64); a bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) enclosed in said housing (See Fig. 3); and a downstream receptacle (i.e., cable connector between lines 136, 138 and lines 90, 94 in Fig. 3) in the housing connected to both said power supply and said bus hub (i.e., line 138 connected to Power Supply 112 and line 136 connected to Protocol Conversion & USB Hub 114 in Fig. 3), said downstream receptacle being coupled to a cable (i.e., line 136 and line 138 in Fig. 3) to couple DC power (i.e., converted 110V AC power to DC; See col. 6, lines 51-54) from said power supply (See col. 6, lines 65-66) and data signals from said bus hub to said cable (See col. 7, lines 11-15) and to receive DC power and data signals from said cable (See col. 6, line 65 through col. 7, line 10). Herwig does not expressly teach said bus hub being coupled to said power supply to receive said DC power from said power supply.

Flannery discloses an apparatus of providing power management using a self-powered USB device (See Abstract and Fig. 1A), wherein said apparatus comprising a power logic 114 (Fig. 1A) and a bus hub (i.e.,

HUB Logic 106 of Fig. 1) being coupled to a power supply (i.e., power supply 108 of Fig. 1A) to receive DC power from said power supply (See col. 5, line 65 through col. 6, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus of providing power management, as disclosed by Flannery, to said apparatus, as disclosed by Herwig, so as to provide a superior solution to supplying the power needs of suspend/resume capabilities in a computer without the inefficiencies of a dual-stage power supply unit or the expense of incorporating both low-power and full-power units (See Flannery, col. 2, line 62 through col. 3, line 2) with the advantage of being able to supply 500mA to each downstream device (e.g., printers and speakers) attached to said bus hub (See Flannery, col. 4, lines 50-64).

*Referring to claim 39*, Herwig discloses a computing unit (i.e., retail terminal system 50 in Fig. 2), comprising: a computer (i.e., main unit 52 of Fig. 2) comprising: an upstream receptacle (i.e., cable connector between line 94 and input device 55 in Fig. 2) to deliver data signals (i.e., USB data signals) to said computer (See col. 7, lines 11-15); and a power receptacle (i.e., cable connector between line 90 and input device 55 in Fig. 2) to deliver electrical power (i.e., terminal power) to said computer (See col. 6, lines 65-67); and a power hub (i.e., wiring Hub 100 of Fig. 3) coupled to said upstream receptacle and said power receptacle of said computer via a cable (i.e., line 136 and line 138 in Fig. 3; See col. 6, line 65 through col. 7, line 10), wherein said power hub (i.e., wiring Hub) comprises: a housing (i.e., housing 110 of Fig. 3); a power supply (i.e., Power Supply 112 of Fig. 3) enclosed in said housing (See Fig. 3), said power supply being coupled to receive alternating current (AC) power (i.e., 110V AC) to convert said AC power into direct current (DC) power (i.e., 5/12 DC; See col. 6, lines 51-64), said power supply being coupled to said cable to provide DC power to said computer (See col. 6, line 65 through col. 7, line 10); and a bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) enclosed in said housing (See Fig. 3), said bus hub being coupled to said cable (i.e., Protocol Conversion & USB Hub 114 of Fig. 3 being coupled to Power & LAN 90 and USB interface 94, viz., cable, in Fig. 2) to receive power (i.e., receiving



Vbus power via USB interface 94 of Fig. 2) and data signals (i.e., receiving D+, D- data signals via USB interface 94 of Fig. 2) from said computer (i.e., main unit).

Herwig does not expressly teach said bus hub being coupled to said power supply to receive DC power from said power supply.

Flannery discloses an apparatus of providing power management using a self-powered USB device (See Abstract and Fig. 1A), wherein said apparatus comprising a power logic 114 (Fig. 1A) and a bus hub (i.e., HUB Logic 106 of Fig. 1) being coupled to a power supply (i.e., power supply 108 of Fig. 1A) to receive DC power from said power supply (See col. 5, line 65 through col. 6, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus of providing power management, as disclosed by Flannery, to said computing unit, as disclosed by Herwig, so as to provide a superior solution to supplying the power needs of suspend/resume capabilities in a computer without the inefficiencies of a dual-stage power supply unit or the expense of incorporating both low-power and full-power units (See Flannery, col. 2, line 62 through col. 3, line 2) with the advantage of being able to supply 500mA to each downstream device (e.g., printers and speakers) attached to said bus hub (See Flannery, col. 4, lines 50-64).

*Referring to claims 30 and 41*, Herwig teaches said bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) comprises a root port (i.e., port from Protocol Conversion & USB Hub 114 for line 136 in Fig. 3).

*Referring to claims 31 and 42*, Herwig teaches said bus hub (i.e., Protocol Conversion & USB Hub 114 of Fig. 3) comprises a downstream port (i.e., USB Port #1 140 and USB Port #2 142 in Fig. 3) to be coupled to a downstream device (e.g., Scanner 66 and POS Keyboard 62 in Fig. 2).

*Referring to claims 32 and 43*, Flannery teaches said bus hub (i.e., HUB Logic 106 of Fig. 1A) is self powered (See col. 5, lines 64-66).

6. Claims 5, 20, 33 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] as applied to claims 1-4, 7, 11, 12, 16, 17, 19, 28-32, 39 and 41-43 above, and further in view of what was well known in the art, as exemplified by USB Specification [Universal Serial Bus Specification published by Compaq, Intel, Microsoft and NEC, Rev. 1.1., September 23, 1998; cited by the Applicant; hereinafter USB Spec].

*Referring to claims 5, 20, 33 and 44*, Herwig discloses all the limitations of the claims 5, 20, 33 and 44, respectively, except that does not expressly teach said bus hub is bus powered.

The Examiner takes Official Notice that said bus hub is bus powered, is well known to one of ordinary skill in the art, as evidenced by USB Spec on page 135, 7.2.1.1 Bus-powered Hubs.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said bus powered bus hub in said apparatus since it would allow power being always available to said bus hub (See USB Spec, 7.2.1.1 Bus-powered Hubs).

7. Claims 6, 18, 34-36 and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] as applied to claims 1-4, 7, 11, 12, 16, 17, 19, 28-32, 39 and 41-43 above, and further in view of Urade et al. [US 6,272,644 B1; hereinafter Urade].

*Referring to claims 6 and 18*, Herwig discloses all the limitations of the claims 6 and 18, respectively, except that does not teach a hub repeater connected to said upstream port.

Urade discloses a USB hub 11 (Fig. 4), wherein a hub repeater (i.e., Hub Repeater 12 of Fig. 4) connected to an upstream port (i.e., Root Port 13 of Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said hub repeater, as disclosed by Urade, in said bus hub, as disclosed by Herwig, as modified by Flannery, so as to manage port connectivity between a selected downstream functional

device and a host computer connected to said upstream port (i.e., root port; See Urade, col. 3, lines 60-62).

*Referring to claims 34 and 45*, Herwig discloses all the limitations of the claims 34 and 45, respectively, except that does not teach a hub repeater coupled between a root port and a plurality of downstream ports in said bus hub to manage connections to and through said bus hub, each downstream port to be coupled to a downstream device.

Urade discloses a bus hub (i.e., USB hub 11 of Fig. 4), wherein a hub repeater (i.e., Hub Repeater 12 of Fig. 4) coupled between a root port (i.e., Root Port 13 of Fig. 4) and a plurality of downstream ports (i.e., Ports 1-4 14-17 in Fig. 4) in said bus hub to manage connections to and through said bus hub (See col. 3, lines 60-64), each downstream port to be coupled to a downstream device (See col. 3, lines 40-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said hub repeater, as disclosed by Urade, in said bus hub, as disclosed by Herwig, as modified by Flannery, so as to manage port connectivity between a selected downstream functional device and a host computer connected to said upstream port (i.e., root port; See Urade, col. 3, lines 60-62).

*Referring to claims 35 and 46*, Urade teaches that said downstream devices comprise a mouse, a keyboard or a printer (e.g., plotter; See col. 3, lines 42-43).

*Referring to claims 36 and 47*, Urade teaches that a hub controller (i.e., Hub Controller 19 of Fig. 4) coupled to said hub repeater (i.e., coupled to Hub Repeater 12 via connection from SIE 20 in Fig. 4) in said bus hub (i.e., USB Hub 11 of Fig. 4) to route signals between said root port and said downstream ports (See col. 3, lines 60-64; i.e., wherein in fact that managing port connectivity between the selected downstream functional device and a host computer connected to the root port implies routing signals between said root port and said downstream ports) and to perform error detection (i.e., error checking) and recovery (i.e., clock recovery; See col. 3, line 65 through col. 4, line 6).

8. Claims 8 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] as applied to claims 1-4, 7, 11, 12, 16, 17, 19, 28-32, 39 and 41-43 above, and further in view of Kang [US 6,253,329 B1] and Tsai [US 6,283,789 B1].

*Referring to claims 8 and 38*, Herwig, as modified by Flannery, discloses all the limitations of the claims 8 and 38, respectively, including said cable (i.e., line 136 and line 138 in Fig. 3; Herwig) comprises a computer power wire (i.e., line 138 of Fig. 4; Herwig) to provide power, which is DC power, from said power supply (i.e., Power Supply 112 of Fig. 3; Herwig) to a computer (i.e., main unit 52 of Fig. 2; See Herwig, col. 6, lines 65-67); and a signal wire (i.e., line 136 of Fig. 3; Herwig) to carry data signals between said computer and said bus hub (See Herwig, col. 7, lines 11-17), except that does not expressly teach a device power wire to provide power to said bus hub; a device ground wire; a computer ground wire; and a plurality of signal wires to carry said data signals.

Kang discloses a USB Hub having a plurality of input power sources (See Abstract and Fig. Fig. 3), wherein a device power wire (i.e., UpStream Vbus in Fig. 3) to provide power to a bus hub (i.e., USB Hub 200 of Fig. 2); a device ground wire (i.e., USB GND wire; in fact, USB UpStream Data Port in Fig. 3 inherently suggests USB GND wire according to the USB specification); and a plurality of signal wires to carry data signals (i.e., USB D+, D- signal wires; in fact, USB UpStream Data Port in Fig. 3 inherently suggests USB D+, D- signal wires according to the USB specification).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said plurality of input power sources, as disclosed by Kang, to said apparatus, as disclosed by Herwig, as modified by Flannery, so as said power supply to supply power to said bus hub for the advantage of providing said bus hub (i.e., USB hub) having a plurality of input power supplies (See Kang, col. 2, lines 3-10).

Herwig, as modified by Flannery and Kang, does not expressly teach a computer ground wire.

Tsai teaches a cable (i.e., cable system 300 of Fig. 1) comprises a device power wire (i.e., wire of cable 15, which is connected to  $V_{bus}$  1a of Fig. 4); a device ground wire (i.e., wire of cable 15, which is connected to GND 4a of Fig. 4); a computer power wire (i.e., wire of cable 16, which is connected to  $V_{bus}$  1a of Fig. 5); a computer ground wire (i.e., wire of cable 16, which is connected to GND 4a of Fig. 5); and a plurality of signal wires (i.e., wires of cable 15, which are connected to D<sub>-</sub> 2a and D<sub>+</sub> 3a in Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said cable, as disclosed by Herwig, as modified by Flannery and Kang, using said cable system, as disclosed by Tsai, for the advantage of providing a compact and clean wiring in said housing, which is a common sense to one of ordinary skill in the art of electronics wiring.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A], Kang [US 6,253,329 B1] and Tsai [US 6,283,789 B1] as applied to claim 8 above, and further in view of Decuir [US 5,781,028 A].

*Referring to claim 9*, Herwig, as modified by Flannery, Kang and Tsai, discloses all the limitations of the claim 9 except that does not teach said plurality of signal wires further comprises a signal twisted pair.

Decuir discloses a system for a switched data bus termination (Fig. 6), wherein a plurality of signal wires (i.e., USB data signal wires in Fig. 6) comprises a signal twisted pair (i.e., twisted pair data cable 72 of Fig. 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said twisted pair cable, as disclosed by Decuir, for said signal wires, as disclosed by Herwig, as modified by Flannery, Kang and Tsai, for the advantage of supporting high speed version of USB (See Decuir, col. 5, lines 5-7).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A], Kang [US 6,253,329 B1] and Tsai [US 6,283,789 B1] as applied to claim 8 above, and further in view of Sanchez [US 6,446,867 B1].

*Referring to claim 10*, Herwig, as modified by Flannery, Kang and Tsai, discloses all the limitations of the claim 10 except that does not teach said plurality of signal wires further comprises a fiber optic channel.

Sanchez discloses an electro-optic interface system (Fig. 2A), wherein a plurality of signal wires (i.e., a plurality of optical links in Fig. 2A), which are driven by a laser module 250 (Fig. 2A) and a photo detector 260 (Fig. 2A), comprises a fiber optic channel (i.e., optical channel of Fiber Optic Cable 135 in Fig. 2A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said fiber optic channel with its driver, as disclosed by Sanchez, for signal wires, as disclosed by Herwig, as modified by Flannery, Kang and Tsai, for the advantage of providing an electro-optic system of operation for communicating high aped digital signals between two or more electronic systems (See Sanchez, col. 1, lines 57-60) without spreading electromagnetic noise, which is well known to one of ordinary skill in the art of fiber optical communication.

11. Claims 13 and 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] as applied to claims 1-4, 7, 11, 12, 16, 17, 19, 28-32, 39 and 41-43 above, and further in view of Tsai [US 6,283,789 B1].

*Referring to claims 13 and 40*, Herwig, as modified by Flannery, discloses all the limitations of the claims 13 and 40, respectively, including said cable (i.e., Power & LAN 90 and USB interface 94, viz., cable, in Fig. 2; Herwig) comprises a device power wire (i.e., Vbus power wire on USB interface 94 of Fig. 2; Herwig) to provide power, which is DC power, from said computer to said bus hub (i.e., bus power on USB interface 94 of Fig. 2; Herwig); a device ground wire (i.e., GND wire on USB interface 94

of Fig. 2; Herwig); a computer power wire (i.e., Power & LAN 90 of Fig. 2; Herwig) to provide power from said power supply to said computer (i.e., main unit 52 of Fig. 2; See Herwig, col. 6, lines 65-67); and a plurality of signal wires (i.e., D+, D- data signal wires on USB interface 94 in Fig. 2; Herwig) to carry data signals (i.e., USB data signals; Herwig) between said computer and said bus hub (See Herwig, col. 7, lines 11-17), except that does not expressly teach a computer ground wire.

Tsai teaches a cable (i.e., cable system 300 of Fig. 1) comprises a device power wire (i.e., wire of cable 15, which is connected to  $V_{bus}$  1a of Fig. 4); a device ground wire (i.e., wire of cable 15, which is connected to GND 4a of Fig. 4); a computer power wire (i.e., wire of cable 16, which is connected to  $V_{bus}$  1a of Fig. 5); a computer ground wire (i.e., wire of cable 16, which is connected to GND 4a of Fig. 5); and a plurality of signal wires (i.e., wires of cable 15, which are connected to D<sub>-</sub> 2a and D<sub>+</sub> 3a in Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said cable, as disclosed by Herwig, as modified by Flannery, using said cable system, as disclosed by Tsai, for the advantage of providing a compact and clean wiring in said housing, which is a common sense to one of ordinary skill in the art of electronics wiring.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] and Tsai [US 6,283,789 B1] as applied to claims 13 and 40 above, and further in view of Decuir [US 5,781,028 A].

*Referring to claim 14*, Herwig, as modified by Flannery and Tsai, discloses all the limitations of the claim 14 except that does not teach said plurality of signal wires comprises a twisted pair.

Decuir discloses a system for a switched data bus termination (Fig. 6), wherein a plurality of signal wires (i.e., USB data signal wires in Fig. 6) comprises a twisted pair (i.e., twisted pair data cable 72 of Fig. 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said twisted pair cable, as disclosed by Decuir, for said signal wires, as disclosed by

Herwig, as modified by Flannery and Tsai, for the advantage of supporting high speed version of USB (See Decuir, col. 5, lines 5-7).

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] and Tsai [US 6,283,789 B1] as applied to claims 13 and 40 above, and further in view of Sanchez [US 6,446,867 B1].

*Referring to claim 15*, Herwig, as modified by Flannery and Tsai, discloses all the limitations of the claim 15 except that does not teach said plurality of signal wires comprises a fiber optic channel. Sanchez discloses an electro-optic interface system (Fig. 2A), wherein a plurality of signal wires (i.e., a plurality of optical links in Fig. 2A), which are driven by a laser module 250 (Fig. 2A) and a photo detector 260 (Fig. 2A), comprises a fiber optic channel (i.e., optical channel of Fiber Optic Cable 135 in Fig. 2A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said fiber optic channel with its driver, as disclosed by Sanchez, for signal wires, as disclosed by Herwig, as modified by Flannery and Tsai, for the advantage of providing an electro-optic system of operation for communicating high speed digital signals between two or more electronic systems (See Sanchez, col. 1, lines 57-60) without spreading electromagnetic noise, which is well known to one of ordinary skill in the art of fiber optical communication.

14. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Tsai [US 6,283,789 B1].

*Referring to claim 21*, Herwig discloses a cable (i.e., Power & LAN 90 and USB interface 94, viz., cable, in Fig. 2) comprising: a device power wire (i.e., Vbus power wire on USB interface 94 of Fig. 2) to provide power from a computer (i.e., main unit 52 of Fig. 2) to a power hub (i.e., wiring Hub 100 of Fig. 2; in fact, bus power on USB interface 94 of Fig. 2); a device ground wire (i.e., GND wire on USB interface 94 of Fig. 2); a computer power wire (i.e., Power & LAN 90 of Fig. 2) to provide power from



said power hub to said computer (i.e., main unit 52 of Fig. 2; See col. 6, lines 65-67); and a plurality of signal wires (i.e., D+, D- data signal wires on USB interface 94 in Fig. 2) to carry data signals (i.e., USB data signals) between said computer and said power hub (See col. 7, lines 11-17), except that does not expressly teach a computer ground wire.

Tsai teaches a cable (i.e., cable system 300 of Fig. 1) comprises a device power wire (i.e., wire of cable 15, which is connected to  $V_{bus}$  1a of Fig. 4); a device ground wire (i.e., wire of cable 15, which is connected to GND 4a of Fig. 4); a computer power wire (i.e., wire of cable 16, which is connected to  $V_{bus}$  1a of Fig. 5); a computer ground wire (i.e., wire of cable 16, which is connected to GND 4a of Fig. 5); and a plurality of signal wires (i.e., wires of cable 15, which are connected to D. 2a and D+ 3a in Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said cable, as disclosed by Herwig, in said cable system, as disclosed by Tsai, for the advantage of providing a compact and clean wiring in said housing, which is a common sense to one of ordinary skill in the art of electronics wiring.

*Referring to claim 22*, Tsai teaches an upstream plug (i.e., B connector 20 and 21 in Fig. 1) to connect to both an upstream bus receptacle and a power receptacle (i.e., peripheral device port system 100 of Fig. 6), wherein said power receptacle draws electric power from said computer power wire (See col. 3, lines 59-63; i.e., wherein in fact that delivering extra power to the peripheral device port system implies said power receptacle draws electric power from said computer power wire).

*Referring to claim 23*, Tsai teaches a downstream plug (i.e., A connector 10 and 11 in Fig. 1) to electrically connect to both a downstream bus receptacle and a power receptacle (i.e., main device port system 200 of Fig. 7), wherein said power receptacle is to supply electric power to said computer power wire (See col. 3, lines 59-63; i.e., wherein in fact that delivering extra power to the peripheral device port system implies said power receptacle is to supply electric power to said computer power wire), and wherein said downstream bus receptacle is connected to said device power wire, said device ground wire,

and said plurality of signal wires (See col. 4, lines 1-11; i.e., wherein in fact that power and data are transmitted by the first cable (e.g., USB cable) between the first port and one of the two ports on peripheral device port system implies said downstream bus receptacle is connected to said device power wire, said device ground wire, and said plurality of signal wires).

15. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Tsai [US 6,283,789 B1] as applied to claims 21-23 above, and further in view of Decuir [US 5,781,028 A].

*Referring to claim 26*, Herwig, as modified by Tsai, discloses all the limitations of the claim 26 except that does not teach said plurality of signal wires comprises a twisted pair. Decuir discloses a system for a switched data bus termination (Fig. 6), wherein a plurality of signal wires (i.e., USB data signal wires in Fig. 6) comprises a twisted pair (i.e., twisted pair data cable 72 of Fig. 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said twisted pair cable, as disclosed by Decuir, for said signal wires, as disclosed by Herwig, as modified by Tsai, for the advantage of supporting high speed version of USB (See Decuir, col. 5, lines 5-7).

16. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Tsai [US 6,283,789 B1] as applied to claims 21-23 above, and further in view of Sanchez [US 6,446,867 B1].

*Referring to claim 27*, Herwig, as modified by Tsai, discloses all the limitations of the claim 27 except that does not teach said plurality of signal wires comprises a fiber optic channel. Sanchez discloses an electro-optic interface system (Fig. 2A), wherein a plurality of signal wires (i.e., a plurality of optical links in Fig. 2A), which are driven by a laser module 250 (Fig. 2A) and a photo detector 260 (Fig. 2A), comprises a fiber optic channel (i.e., optical channel of Fiber Optic Cable 135 in Fig. 2A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said fiber optic channel with its driver, as disclosed by Sanchez, for signal wires, as disclosed by Herwig, as modified by Tsai, for the advantage of providing an electro-optic system of operation for communicating high speed digital signals between two or more electronic systems (See Sanchez, col. 1, lines 57-60) without spreading electromagnetic noise, which is well known to one of ordinary skill in the art of fiber optical communication.

17. Claims 37 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herwig [US 6,701,192 B1] in view of Flannery [US 5,799,196 A] and Urade [US 6,272,644 B1] as applied to claims 6, 18, 34-36 and 45-47 above, and further in view of Silverman et al. [US 6,370,603 B1; hereinafter Silverman].

*Referring to claims 37 and 48*, Herwig, as modified by Flannery and Urade, discloses all the limitations of the claim 37 and 48, respectively, except that does not expressly teach said hub controller and said hub repeater comprising memory stored instructions executable by a processor or logic gates or a programmable logic device.

Silverman discloses a configurable universal serial bus (USB) controller (See Abstract and Fig. 4), wherein a hub controller and a hub repeater (i.e., Serial interface engine 412 and USB interface 414 in Fig. 4) comprising memory stored instructions (i.e., user's program in Flash memory 406 in Fig. 4) executable by a processor (i.e., 16-bit processor 404 of Fig. 4; See col. 6, lines 59-61), logic gates (e.g., timer logics 405a and 405b in Fig. 4) and a programmable logic device (i.e., PLD/FPGA 416 of Fig. 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration components (i.e., user's program in Flash memory run by 16-bit processor, timer logics and PLD/FPGA), as disclosed by Silverman, in said hub controller and said hub repeater, as disclosed by Herwig, as modified by Flannery and Urade, for the advantage of providing an

improved technique for effecting digital communications between said downstream devices (i.e., digital devices) and systems using different communication protocols (See Silverman, col. 4, lines 10-13).

***Response to Arguments***

18. Applicant's arguments filed on 18<sup>th</sup> of June 2004 have been fully considered but they are not persuasive.

*In response to the Applicant's argument with respect to* "Herwig issued on 2 March 2004, which is after the filing date of the present application. The applicant does not admit that Herwig is prior art, ..." on Response page 10, lines 16-19, the Examiner notices that the Applicant fails to file 37 CFR 1.131 affidavit or declaration of prior invention in order to overcome the claims 1-3, 11, 12, 16 and 17 rejections under 35 USC § 102(e) by swearing back of the reference Herwig through said 37 CFR 1.131 affidavit or declaration of prior invention.

Thus, the Applicant's argument on this point is not persuasive.

*In response to the Applicant's argument with respect to* "The Office Action cites the Universal Serial Bus Specification, Revision 1.1, page 136, in support of this rejection. Office Action, page 4. The applicant respectfully submits that page 136 of the USB Specification is not of record and no copy of it was provided (see MPEP 707.05(a)). The applicant respectfully requests that the reference be made of record with a copy being provided to the applicant, or that the rejection be withdrawn. ..." on Response page 11, lines 14-28, the Examiner notices that the Applicant cited USB Specification, Revision 1.1, in the IDS filed on 12<sup>th</sup> of March 2001. Thus, this reference was in the record when the Examiner cited this reference in the Office Action mailed on 13<sup>th</sup> of April 2004.

If the Applicant didn't have the copy of Universal Serial Bus Specification, Revision 1.1., the Examiner doubts how the Applicant could cite the specific pages 17 and 230 of the reference, Universal Serial Bus Specification, Revision 1.1 when the Applicant filed the IDS.

Thus, the Applicant's argument on this point is not persuasive, however, the Examiner attaches the copy of the reference Universal Serial Bus Specification, Revision 1.1., pages 135 and 136 for the convenience of the Applicant.

*In response to the Applicant's argument with respect to "...The Office Action has not cited evidence of record in support of this motivation to modify Herwig as is required by In re Vaeck, and In re Lee. Furthermore, the applicant notes that Herwig has a priority date of 13 September 2000, well after the September 1998 publication of the USB Specification, Revision 1.1. Even though the USB Specification cited was available to Herwig, Herwig does not show the feature alleged to be 'obvious' in the Office Action. ..."* on Response page 12, lines 1-13, and the similar arguments on Response page 16, lines 1-18, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, MPEP 706.02(j) clearly states "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. ...".

Moreover, the establishing a *prima facie* case of obviousness in order to show the obviousness of the claimed invention is not proposed by the reference inventor, i.e., Herwig, but by the one of ordinary skill in the art. In other words, the reference Herwig is not necessary to show the feature to be 'obvious' in the Office Action. See MPEP 706.02(j).

Thus, the Applicant's argument on this point is not persuasive.

19. Applicant's arguments with respect to claims 6-10,13-15 and 18 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Russel [US 6,584,519 B1] discloses extender for universal serial bus.

Dunn et al. [US 6,735,720 B1] disclose method and system for recovering a failed device on a master-slave bus.

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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